GOSSIPO-3: Measurements on the Prototype of a Read-Out Pixel Chip for Micro-Pattern Gas Detectors

Abstract - 100/100 words

GOSSIPO-3 is the demonstrator of a front-end chip for the read-out of Micro Pattern Gas Detectors designed in IBM130nm CMOS in collaboration of Nikhef and the Physics Institute Bonn.

The prototype features charge sensitive amplifiers, discriminators, high resolution Time to Digital Converter, Low Drop Out regulators for supply voltage control of the TDC, biasing circuits and control logic on a $2x1mm^2$ die. It can be operated in a time measuring or an event counting mode. Following the prototype announcement at TWEPP2009, measurement data on noise performance, channel to channel gain, ToT spread and LDO load step response are now available.

Summary - 499/500 words

Shortly after its announcement at TWEPP2009 in Paris, GOSSIPO-3 entered production. GOSSIPO-3 is a prototype of a front-end pixel chip for position-sensitive Micro Pattern Gas Detectors with $60x60\mu m^2$ pixels for high granularity. The front-end demonstrator can operate in 24bit event counting mode or in time recording mode allowing measurements with a target precision of 1.7ns (bin size) and a dynamic range of 102µs the for arrival time. The target specifications for the Time over Threshold (ToT) measurements are an accuracy of 25ns (corresponding to sigma=200e⁻) and a ToT range of up to 6.4µs. The target noise performance of the Charge Sensitive Amplifier (CSA) is ENC=70e⁻ (input equivalent) and a rise time of less than 20ns. The goal for the power consumption is $3\mu W$ /channel. The chip has been implemented in close collaboration of Nikhef (Amsterdam) and Physics Institute Bonn (Bonn). The chip is designed in an 8 metal layer IBM 130nm standard CMOS technology available through MOSIS.

The demonstrator comprises a complete pixel cell with analogue front-end circuits including biasing plus an on-pixel high resolution Time to Digital Converter (TDC), counters and control. The frequency of the ring-oscillator in the TDC can be tuned by regulating the supply voltage of the Voltage Controlled Oscillator (VCO). This is done with the help of a Low Drop-Out voltage regulator (LDO). Two alternative circuits for this LDO have been implemented. In addition to these circuitries, three CSAs with constant current feedback each followed by a discriminator have been implemented. The CSAs share a common charge injection pad for testing. The outputs of all three discriminators are externally available through buffers. The comparator thresholds can be globally tuned on-chip by a 4-bit Digital to Analogue Converter. One of the CSA outputs is also buffered and available on a test pad. Besides these pixel related circuits, there is an InGrid Preamplifier (IP) on the demonstrator. When the final front-end chip is used in gaseous detectors with InGrid electron amplification stage, the IP is meant to deliver valuable information on charge injections on the amplifying grid. The inputs of the CSAs are protected from high-voltage breakdown between chip surface and InGrid by an especially designed protection device and a SiNitride protection layer on top of the die. The "S3 Multi IO Board" designed by Physics Institute Bonn and well-known in the pixel detector community is used for the read-out of the digital counter logic.

First measurements on the preamplifier indicate a noise performance of the CSA well below ENC=70e⁻. First ToT measurements show good linearity but a channel-to-channel spread of about 45%. On-going analyses trace the fluctuation back to variations of the discharge feedback current of the CSA.

Both LDO test circuits take less than 5ns to re-settle (accuracy 2%) after a current load step of 20mA which is expected to be the average load step from average to peak activity for a detector consisting of 256x256 pixels with 240 active pixels per bunch crossing. In autumn 2010 further measurement results and analyses will be available.

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