A power scalable 10-bit pipeline ADC for Luminosity Detector at ILC

Marek Idzik, Krzysztof Swientek, Tomasz Fiutowski, Szymon Kulis, Prasoon Ambalathankandy

***Abstract*—The design and measurement results of a power scalable 10-bit pipeline ADC developed for the luminosity detector at the future International Linear Collider (ILC) are discussed. The prototype is designed and fabricated in 0.35 μm CMOS technology. A wide spectrum of measurements of static (INL$<$1 LSB, DNL$<$0.5 LSB) and dynamic (SNHR$>$58 dB, SINAD $\sim$58 dB) parameters are performed to understand and quantify the circuit performance. The ADC works for sampling rates from 1 kS/s to 25 MS/s covering more than four orders of magnitude. In most of the range power consumption scales linearly with sampling rate with a factor of 0.85 mW/MS/s.**

***Index Terms*—Pipeline ADC; Power scaling; Fully differential amplifier; Dynamic latch comparator; Power switching.**

I. Introduction

In the future International Linear Collider (ILC) luminosity will be measured by the LumiCal, a dedicated detector in the Forward Calorimetry region [1]. The LumiCal will be a Si/W sandwich calorimeter composed of interleaved layers of passive absorber (W) and active sensor (Si). The signals from silicon sensors, radially segmented around the beam, will be processed and digitised by a dedicated multichannel front-end electronics [2], [3] and subsequently sent to a following part of the readout system. In total the LumiCal will consist of about 200,000 readout channels. The Monte Carlo simulations indicate that about a 10-bit resolution is needed by the reconstruction procedure to measure the energy deposited in the calorimeter [4]. Considering the requested number of channels and the limitations on space and power dissipation, a signal digitisation needs to be performed by a dedicated multichannel ADC. Initially two analog to digital conversion schemes were considered: one with relatively slow ADC per each channel and one with faster ADC per group of about 8 channels. The first option would simplify the overall design scheme, while the second would allow to save on area. The first option requires an ADC with a sampling rate of about 3 MS/s while the second one needs a sampling rate of about 24 MS/s. These different conversion schemes were a main motivation for the development of a variable sampling rate ADC with scalable power consumption. In addition, the ADC with scalable sampling rate and power can be very useful in other blocks of readout system requiring analog to digital conversion. A typical application is a temperature and power supply monitoring. A very important consideration in the ADC design is to take advantage of the ILC beam timing structure, which consists of about 1 ms long active beam followed by about 200 ms pause [5]. Applying a power switch off during the beam pause will allow operation with a very low average power consumption, and so will facilitate fulfiling demanding power consumption requirements. It is well known that one of the most efficient ADC architectures assuring a good compromise between the sampling rate, power consumption and area, is the pipeline ADC [6], [7], [8]. Such architecture is chosen in this work.

The paper is organised in two parts. In the first part the ADC design and the implementation of key circuit blocks are presented. The second part describes the measurements performed on the prototype ADC with the obtained results.

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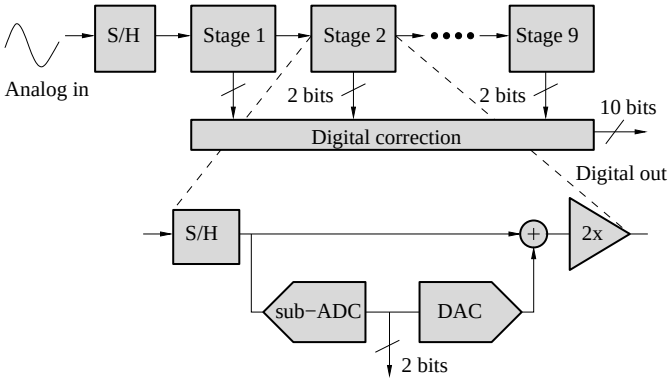


Fig. 1. Pipeline ADC architecture.

II. ADC architecture and design

A. ADC architecture

The choosen ADC architecture is shown in figure 1. The ADC is built of sample and hold input stage and nine serially connected 1.5-bit pipeline stages. The digital correction block creates a 10-bit output code using the redundant signed digit (RSD) principle [9]. A 1.5-bit stage architecture is chosen because of its simplicity and immunity to the offsets in the comparator and amplifier circuits [6]. To improve the immunity to digital crosstalk and other disturbances, each ADC stage is implemented using a fully differential architecture. The reference voltages are applied externally to the ADC.

A simple unity gain stage is used as a sample and hold (S/H) circuit. Its block diagram is shown in figure 2. It samples the

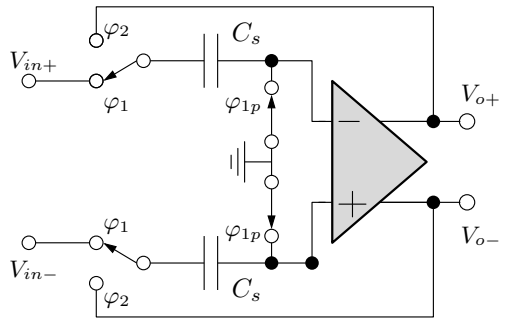


Fig. 2. Simplified schematic of a sample and hold stage. Switches set to sampling phase φ_1.

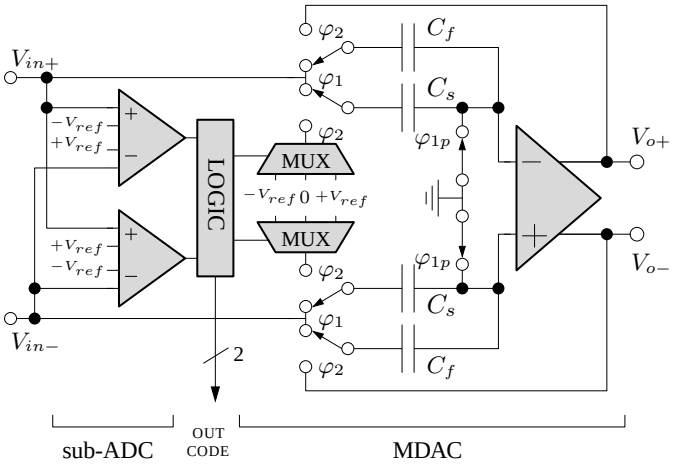


Fig. 3. Simplified schematic of a 1.5-bit stage. Switches set to sampling phase φ_1.

input signal in the sampling phase φ_1 and delivers it to the output in the hold phase φ_2. In order to decrease the sampling resistance and make it independent on signal amplitude a bootstrapped MOS switch (bewteen $V_{in\pm}$ and C_s) described in [10] is implemented in the S/H input. The additional copy φ_{1p} of φ_1 clock (see fig. 6) with a slightly advanced falling edge is used to avoid charge injection at the end of sampling phase, by the means of a so called bottom plate sampling configuration.

The block diagram of a single 1.5-bit stage is shown in figure 3. It consists of a multiplying digital-to-analog converter circuit (MDAC consisting of operational transconductance amplifier, two pairs of capacitors C_s, C_f and several switches) and a sub-ADC circuit (two comparators and small digital logic circuit). The operation of this stage is performed in two phases. In phase φ_1 (shown in fig. 3) capacitors C_s and C_f are connected between $V_{in\pm}$ and ground (in reality to common voltage V_{cm}, i.e. AC ground) and charged to voltages $V_{in\pm}$. In phase φ_2, capacitors C_f are in the amplifier feedback while capacitors C_s are connected to the DAC reference voltages ($\pm V_{ref}$ or 0 depending on comparators decisions). Assuming infinite amplifier gain, the transfer function (in single ended version) of one pipeline stage is given by the formula:

$$V_o = \left(1 + \frac{C_s}{C_f}\right) V_{in} - \frac{C_s}{C_f} V_R,$$
$$V_R = \begin{cases} -V_{ref} & V_{in} < th_{\text{low}} \\ 0 & th_{\text{low}} < V_{in} < th_{\text{high}} \\ V_{ref} & V_{in} > th_{\text{high}} \end{cases}, \quad (1)$$

where $C_f = C_s$, $th_{\text{low}} = -1/4V_{ref}$, $th_{\text{high}} = 1/4V_{ref}$.

The first eight pipeline stages have the same architecture, differing only in values of capacitances C_s, C_f and in currents drawn by the amplifiers. The 9th stage contains only the sub-ADC circuit since multiplication is not required in the last stage.

B. Fully differential amplifier

The key block of a pipeline ADC stage is a transconductance differential amplifier. A telescopic cascode amplifier configuration is used here since, compared to commonly used configurations i.e. folded cascode or two stage amplifier, it represents the most efficient solution for speed versus power. The chosen technology with relatively high (3.3 V) supply voltage gives enough voltage range for the correct biasing of the stack of 5 transistors required by telescopic configuration. The block diagram of the implemented fully differential amplifier with a common-mode feedback (CMFB) circuit is shown in figure 4. To obtain smaller power consumption, and to allow power scaling in a large biasing range, a switched-capacitor CMFB is implemented in this work. In order to obtain a high enough gain in a one stage amplifier, a gain-boosting cascode scheme is implemented [11], [12]. The gain boosting is implemented

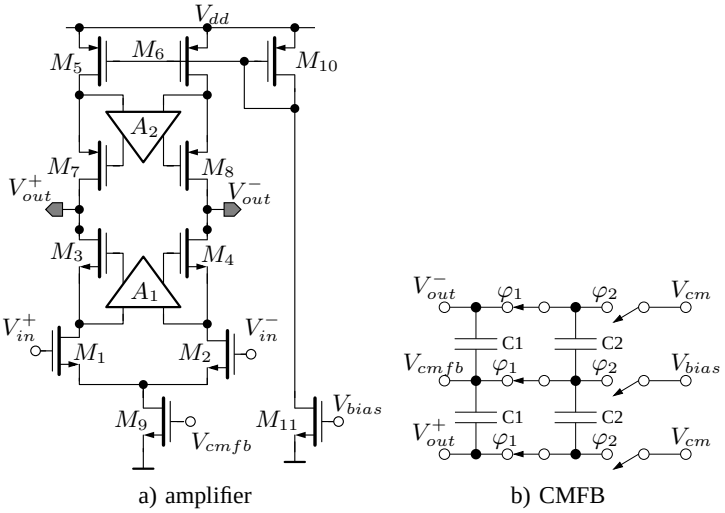


Fig. 4. Block diagram of the fully differential amplifier with boosted gain on the left and SC CMFB circuit on the right.

in the lower and the upper cascode branches by the amplifiers A_1 and A_2. Both boosting amplifiers are fully differential single stage amplifiers with switched-capacitor CMFB circuit similar to the main amplifier. The lower branch amplifier (A_1) uses a telescopic cascode configuration while the upper branch amplifier (A_2) uses a folded cascode configuration with NMOS input transistors. The DC value of the amplifier's

outputs are controlled by an externally applied common mode potential V_{cm}. The simulation shows above 100 dB open loop gain and about 70° phase margin, which leaves a large margin for the requested 10 bit resolution ADC. The amplifier power consumption is scaled in the subsequent pairs of ADC pipeline stages decreasing the bias current by a factor of about 0.7 every two stages.

The ADC power switching off feature is implemented by adding the possibility of switching on or off the biasing currents of amplifiers.

C. Dynamic latch comparator

Since the 1.5-bit stage architecture leaves very relaxed requirements on the comparators threshold (∼100 mV precision for V_{ref} of about 1 V) a simple dynamic latch architecture can be used. For this work the circuit proposed in [13] is choosen, which for completness, is shown in figure 5. The

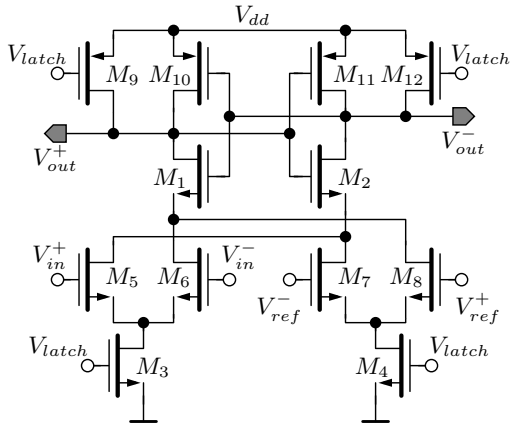
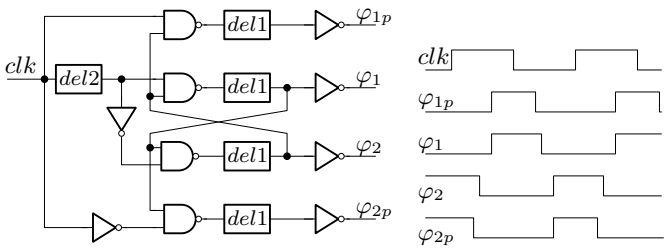


Fig. 5. Block diagram of the dynamic latched comparator.

choice is motivated by a particularly good insensitivity to transistor mismatch and input signal common mode value. A small inconvenience is the fact that the threshold in this implementation is not given by a simple ratio of transistor size but is given by a second order equation [13].

D. Clocks generation

For correct operation of pipeline stages, two nonoverlaping clocks φ_1 and φ_2 are generated to control the sampling and multiplying phase. The clocks generator, shown in figure 6,



a) generator b) diagram

Fig. 6. Block diagram of clock generator and diagram of generated nonoverlaping clocks.

is similar to the one used in [14]. In this implementation, the nonoverlaping time may be changed by an externally controlled delay $del1$. Two additional copies φ_{1p}, φ_{2p} of φ_1, φ_2 with slightly advanced falling edges are generated to avoid charge injection in the sampling phase. This short delay between the falling edges may be changed by an externally controlled delay $del2$.

III. Measurement results

The prototype ASIC is fabricated in a 0.35 μm, four-metal two-poly CMOS technology. The picture of the ASIC containing few ADC prototypes, glued and bonded on PCB is shown in figure 7. The active size of the ADC is 0.3×2.9 mm. For each ADC channel the S/H stage and 9 pipeline stages are layout in series, while the digital logic and correction are placed in parallel to analog blocks.

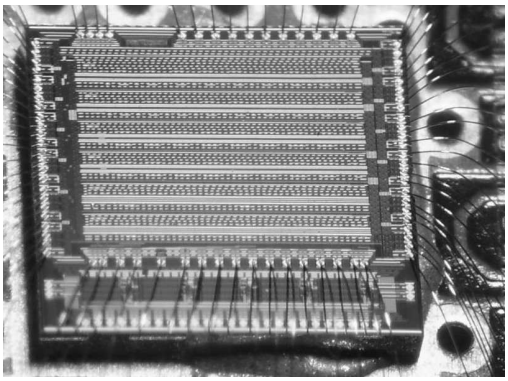


Fig. 7. Photograph of glued and bonded prototype ASIC.

To facilitate the tests a dedicated FPGA based test setup was developed [15]. After the initial tests of a basic functionality with a DC input signal, the complete measurements of ADC static and dynamic parameters are performed. In the next step, a power consumption scaling as a function of sampling frequency is studied. Finally the power switching off feature is tested and the ADC performance is summarized and compared to other works.

A. Static INL & DNL measurements

The static measurements are performed at various sampling frequencies and with the input voltage ramped in the range from -1 V to 1 V. To eliminate noise, the measurements are repeated several tens of thousand of times. An example of the ADC transfer function measured at sampling frequency of 10 MHz is plotted in figure 8, showing a full ASIC functionality and linearity in first approximation.

The ADC performance is quantified with the integral nonlinearity (INL) and the differential nonlinearity (DNL) measurements. Both parameters are obtained with the histogramming method [16]. Typical results are shown in figure 9. The measured INL is less than 1 LSB while the DNL is less than 0.5 LSB. Both parameters stay within the specification for 10-bit resolution.

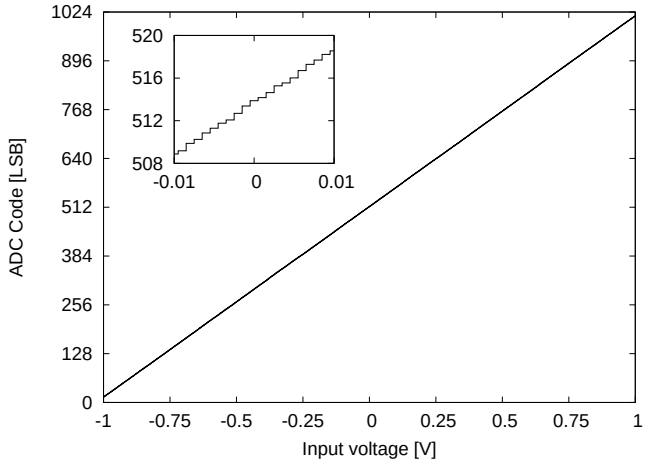


Fig. 8. ADC transfer function measured at 10 MHz sampling frequency.

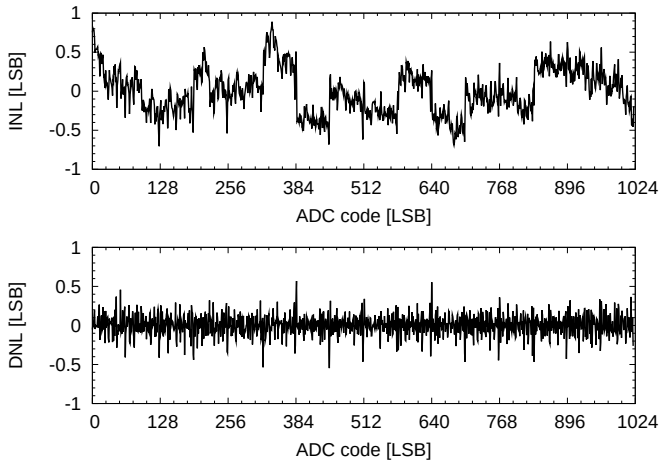


Fig. 9. INL and DNL measured at 10 MHz sampling frequency and calculated using the histogramming method.

B. Dynamic FFT measurements

To evaluate dynamic circuit performance, Fast Fourier Transform (FFT) spectrums are calculated from the measurements done with a sinusoidal input signals [16]. The standard ADC metrics i.e. the Signal to Non Harmonic Ratio (SNHR), the Total Harmonic Distortion (THD) ratio, the Spurious Free Dynamic Range (SFDR) and the Signal to Noise and Distortion Ratio (SINAD) are calculated to quantify the ADC dynamic performance. An example of FFT spectrum measurement for a 0.49 MHz full scale (0 dB) input signal sampled at 10 MS/s is shown in figure 10. The obtained dynamic parameters values of SNHR, THD, SFDR and SINAD are typical for a wide range of sampling and input frequencies. Such performance with the SINAD $\sim$58 dB corresponds to the effective number of bits (ENOB) of about 9.3.

The dependence of dynamic FFT metrics on ADC sampling frequency is shown in figure 11. The two plots show the dynamic metrics obtained for the input frequency 1/10 of sampling frequency (up) and around the Nyquist input frequency (down). One may conclude that the ADC performs well (good SNHR) for sampling frequency up to about 25 MHz. Above

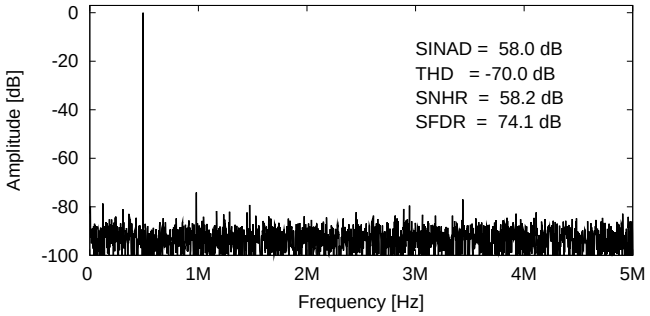


Fig. 10. Example FFT measured for 0.49 MHz input frequency at 10 MHz sampling frequency.

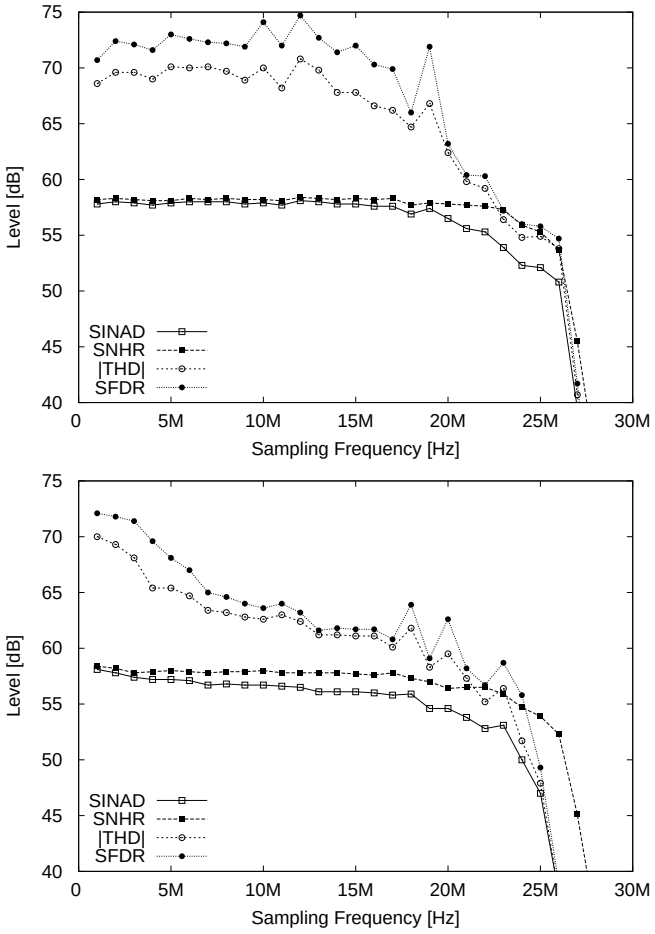


Fig. 11. ADC dynamic performance as a function of sampling rate obtained with input signal signal frequency 1/10th of sampling frequency (up) and at Nyguist frequency (down).

this frequency the performance drops due to the bandwidth limitation of the MDAC amplifier. For lower input frequencies the signal to noise ratio (SINAD) is about 58 dB in most parts of the sampling frequency range, as seen in figure 11 (up). For input frequencies around the Nyquist rate, shown in figure 11 (down), the obtained results are generally 1–2 dB lower because of harmonic distortions (THD). It is not clear whether this decrease of the THD (and so the SINAD) should be attributed to the ADC or rather to the signal generator (Tektronix AFG3102). According to the AFG3102 specifications its

harmonics deteriorate significantly above 1 MHz and in fact such effect is observed in both plots of figure 11, suggesting that the ADC performance may be better than shown in these plots.

The dependence of dynamic ADC metrics on input signal frequency is shown in figure 12 for sampling frequency equal 10 MHz. A good almost flat behaviour of the SNHR is

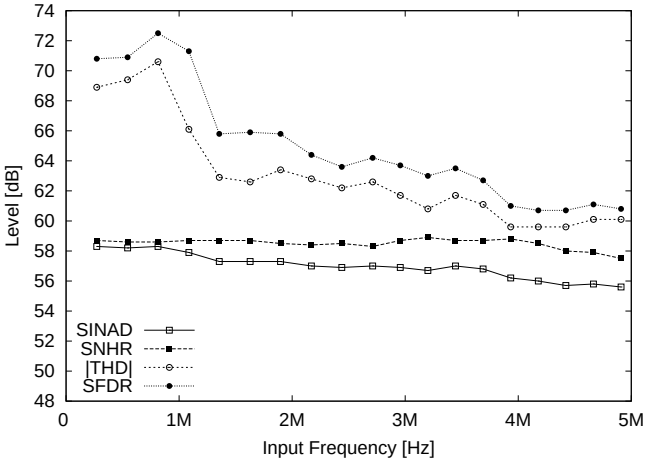


Fig. 12. ADC performance as a function of input signal frequency at 10 MHz sampling frequency.

observed over the whole Nyquist band. The SINAD decreases from ∼58 dB to about 56 dB at Nyquist frequency. As mentioned before the origin of this decrease is not clear. The measurements were done also for the input frequency above the Nyquist band and it was verified that the SNHR is almost flat up to twice the sampling frequency.

C. Power scaling

The ADC power consumption is scaled changing simultanously the bias currents in all amplifiers. To find an optimum bias, for each sampling frequency the minimum bias current guaranting the SNHR of 58 dB (slightly less for sampling frequecies close to 25 MHz), is selected. The measured power consumption versus sampling frequency is shown in figure 13. The two curves showing the ADC power consumption are measured with and without including the output buffers (each output buffer is loaded with several pF). The third curve shows the bias current setting. For better visibility, the power consumption results normalized to 1 MS/s sampling rate are also shown (lower plot). The results shown in figure 13 are obtained around Nyquist input frequency. The measured power consumption contains the ADC analog and digital power but does not include the external reference voltages power. A few observations can be made from looking at the results shown in figure 13:

- The ADC core power consumption scales over more than 4 orders of magnitude from about 1 μW to 34 mW. In most of this range, i.e., in almost 4 orders of magnitude, power cosnumption scales linearly with sampling frequency.
- In the region of linear scaling the ADC core consumes about 0.85 mW/MS/s.

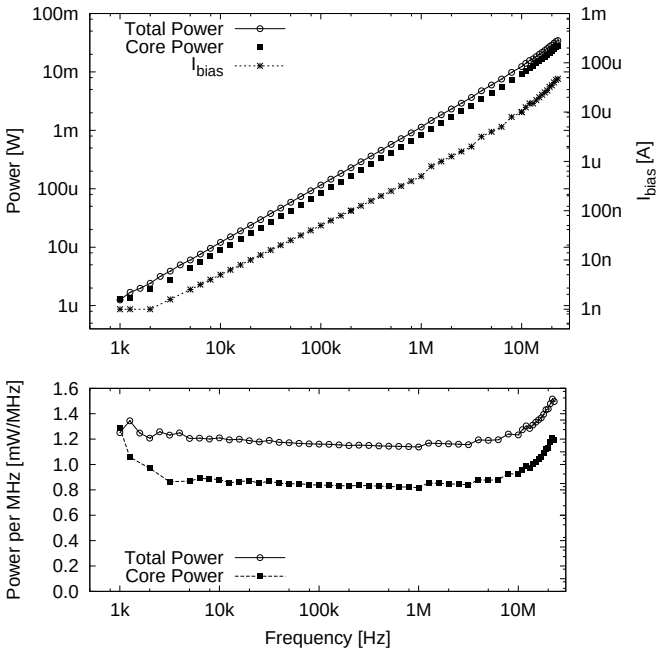


Fig. 13. ADC power scaling, V_{supp}=3 V.

- The optimum bias setting is rather simple since the optimum bias current scales similarly to power consumption.

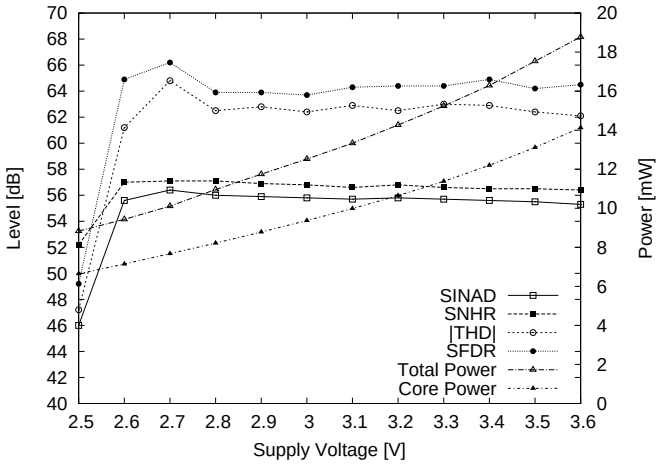


Fig. 14. ADC dynamic performance and power consumption as a function of supply voltage at 10 MHz sampling frequency and around Nyquist input frequency.

In order to check the possibility of further minimization of power consumption and to get an idea about the possibility of scaling the design to smaller size technologies, the ADC dynamic performance and power consumption are measured as a function of supply voltage. The resulting dynamic parameters and power consumption obtained around Nyquist input frequency for 10 MHz sampling frequency are shown in figure 14. It is seen that the ADC works without parameter deterioration for supply voltages down to about 2.6 V. At the 2.6 V supply the power consumption of the ADC core is about 2/3 compared to the measurements shown before (obtained at 3 V power supply). It means that the minimum ADC core

power consumption can be lowered below 0.6 mW/MS/s, and it is a good indication regarding scaling the design to smaller technology.

D. Switching off power

As mentioned in the introduction, a very important feature helping limiting power consumption in the future linear collider will be the possibility of switching off the power during the beam pause. This feature is studied measuring the transient times necessary for switching on the bias currents in the prototype ADC. Figure 15 shows the measurements of the ADC output versus the time passed from the switching on instance and expressed in the number of sampling clock periods, performed for different sampling frequencies. The curves seen in figure 15 are obtained for different sampling frequencies applying a triangular signal to the ADC input. Depending on

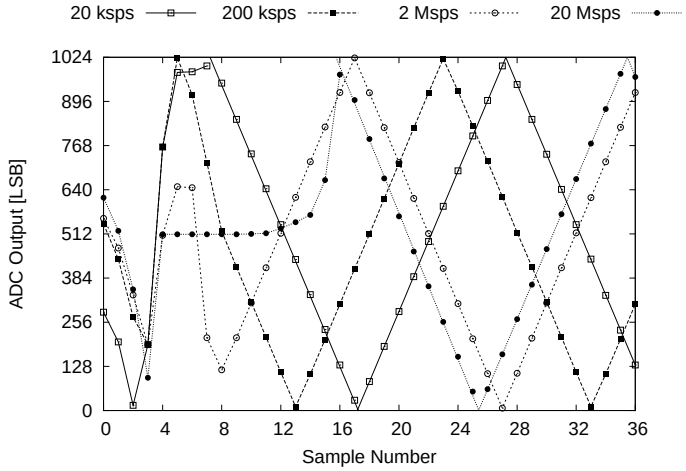


Fig. 15. ADC output versus sample number after power switching on.

ADC sampling frequency between 8 and 16 clock periods are needed to restart the correct data conversion. For the ILC case (about 300 ns period between beam crossings) it would take about 3 μs to return to proper operation, which is a negligible part of the pause (200 ms).

E. Comparison to other ADC

It is rather difficult to find a power scalable ADCs in the literature since typically ADCs are optimized for a given sampling frequency. One of the very few exceptions published in recent years is described in [17]. The comparison of the key parameters obtained in this work and found in [17] is shown in table I. The compared design [17] is slightly more power efficient (compared to 0.85 mW/MS/s in this work) at higher sampling rates, while significantly less efficient at low sampling rates. It should be noted that design [17] was impemented in a smaller size and lower power supply technology, and its power consumption does not cover the digital correction circuit and output buffers. This work performs slightly better in both static and dynamic tests and occupies less area. The authors of [17] have published recently a new version of a power scalable ADC [18] which is about 20% more efficient than their previous design (0.6 mW at 164 KS/s, 27 mW at 50 MS/s). It is not included in table I since the minimum sampling rate of the ADC presented in [18] equal 164 kS/s is more than 2 orders of magnitude higher compared with ASICs from table I.

IV. Conclusion

In this paper the design and measurements of a power scalable 10-bit pipeline ADC are presented. The prototype ADC occupies 0.87 mm^2. The ASIC is fully functional and the performed measurements confirm a good static (INL$<$1 LSB, DNL$<$0.5 LSB) and dynamic (SINAD $\sim$58 dB) performance, which is reflected in a high effective number of bits, ENOB=9.3. The ADC operates for sampling frequencies from 1 kHz to 25 MHz and the power consumption scales linearly with the sampling frequency over most of this range (almost 4 orders of magnitude). This feature makes the ASIC very flexible allowing its use as a general purpose ADC. The scalable power, together with a relatively small area (and pitch), extends the range of possible applications making the design very attractive for multichannel circuits. The possibility of switching off the power improves the average power consumption efficiency even more in applications with long idle times (like ILC). In summary, the ADC fulfills the requirements and is ready to be implemented in the multichannel readout of the LumiCal detector.

Acknowledgments

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TABLE I
COMPARISON WITH OTHER ADC

	This work	[17]
architecture	10-bit pipeline	10-bit pipeline
technology	0.35 μm CMOS	0.18 μm CMOS
sampling rate range	1 kS/s–25 MS/s	1 kS/s–50 MS/s
input range	2 V_{pp}	1.6 V_{pp}
power consumption	$\sim$0.85 mW/MS/s, 3 V_{supp} ($\sim$0.6 mW/MS/s, 2.6 V_{supp})	15 μW at 1 kS/s, 35 mW at 50 MS/s, 1.8 V_{supp}
area	0.87 mm^2	1.2 mm^2
linearity	INL $<$ 1 LSB, DNL $<$ 0.5 LSB	INL $\leq$ 1.2 LSB, DNL $<$ 1 LSB
SINAD	56–58.5 dB	54–56 dB

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