

Tests of monolithic CMOS SOI pixel detector prototype INTPIX3

by

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Test and Measurement of CMOS SOI(Silicon-On-Insulator) Monolithic Pixel Detector INTPIX3

Introduction: SOI technology allow us to use thick and thin high resistivity Si and Low-resistivity Si respectively on the same processed wafer. The advantages of this technology are less parasitic capacitance, higher speed and low power consumption. This technology does not require bump-bonding and allows a construction of low cost and thin pixel detector. SOI process is expected to be radiation hard.

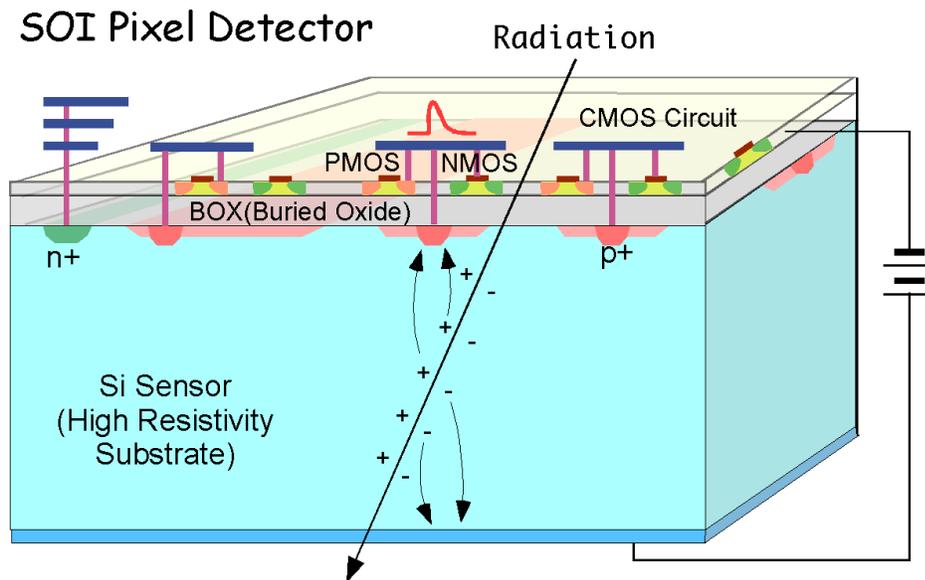


fig1: Schematics of SOI Monolithic Pixel Detector

INTPIX3: INTPIX3 is a pixel detector prototype committed in the 2009 MPW run, designed by Y. Arai (KEK, Japan), to study remedies to back-gate effect observed in previous prototypes. It is a signal integration type pixel detector, fabricated with OKI SOI 0.2 μm process. The pixel size is $20 \times 20 \mu\text{m}^2$ and the total number of pixels on the chip is 16384 (128 \times 128). Each pixel has integration-type sensor circuit. Layout area is $5 \times 5 \text{ mm}^2$. Thickness of the wafer is 260 μm with Al-spattering with thickness of 200nm applied on back side.

The Buried P-Well (BPW) implantation layer, seen under BOX(Buried Oxide) in fig1, was introduced to suppress the back gate effect which was observed in previous prototypes. Eight different layouts are included in INTPIX3 chip to evaluate the back-gate effect and its suppression,. The layouts differ by the presence of the BPW, its area and shape or shape of the p+ implant. The size of each layout is (64 \times 32) pixels, fig2 shows the INTPIX3 pixel blocks.

The details of pixel blocks are as follows:

1. Only one p+ BPW and double external BPW ring
2. One p+ BPW and single external BPW ring
3. One p+ and single external BPW ring with one p+ not connected to BPW
4. INTPIX2 type layout with four P+ without BPW
5. INTPIX2 type layout with slightly smaller BPW
6. INTPIX2 type layout with BPW
7. One p+ with BPW
8. INTPIX2 type layout with four P+ with BPW, but transistors are not covered by BPW.

1 1pBPW+ 2Ex.BPW	2 1pBPW+1Ex.BPW
3 1Ex.BPW	4 INTPIX2 (4p)
5 4pBPW (2um edge)	6 4pBPW (1um edge)
7 1pBPW	8 4pBPW Tr. are not covered

fig2: INTPIX3 Pixel Blocks

Measurements: Various measurement were done with INTPIX 3 prototype to study the back-gate effect:

1. Detector Leakage Current vs Back Voltage characteristic.
2. Measurements of pedestal shift in each of the 8 regions with different guard ring voltages.
3. Dependence of the transistors characteristics on the back voltage.
4. Test of response of the detector to red light diode (650 nm).
5. Irradiation of INTPIX3 with Americium Am-241.

1. **Detector Leakage Current vs Back Voltage characteristic:**

Measurement is shown in I-V Characteristic. The breakdown voltage is 130 V. Theoretical calculation : the detector diode back voltage applied yields the depletion depth which can be obtained from the following formula:

$$W_{calc} = \sqrt{2\varepsilon_S(V_{bi} + V_{back})\rho\mu_n} = \sqrt{\frac{2\varepsilon_S(V_{bi} + V_{back})}{qN_B}}$$

μ_n : electrons mobility

ε_S : silicon permittivity

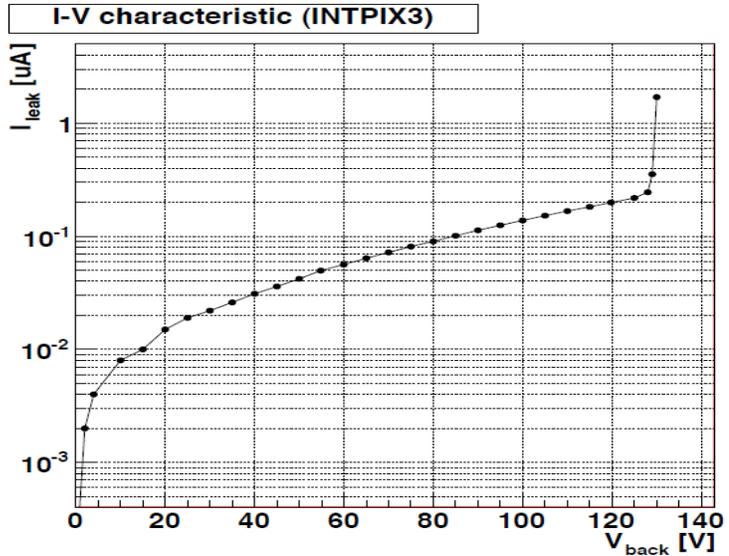
N_B = doping

V_{bi} = V built-in = 0.5V

ρ = Resistivity = 700Ωcm

It is seen that the depletion layer at 130 V is about 160 micrometers. The planned Belle II experiment pixel detector thickness is 50-75 micrometers, thus the properties of INTPIX3 (after thinning) meet requirements of the detector.

$V_{back}(V)$	$W_{dep}(\mu m)$
0	10
10	45
20	64
30	78
50	100
100	141
120	154
200	199
250	223
300	244



2. Measurements of pedestal shift in each of the 8 regions with different guard ring voltages:

The analysis of pedestal shift is done in the readout test bench, based on the SEABAS readout board. A set of macros in c++ using Root was written to analyze the data. This sensor consist of 8 regions out of which first three regions(1,2, and 3) are with guard ring(guard voltages), which surrounds the detector diode to isolate it from the edge of the wafer (mechanical damages at the edge from wafer cutting lead to additional large leakage currents). The guard ring, biased at the same potential as the detector electrode, captures the edge currents and also forms a well-defined electrical boundary for the detector diode. The region 4 is without BPW layer and suffers from the back gate effect. Other four regions are with BPW of differing BPW area shape and size.

The test setup for fig3 is as follows:
 Integration time is 10us
 V_{back} is 5V with 10 steps
 Reset Voltage is 660mV

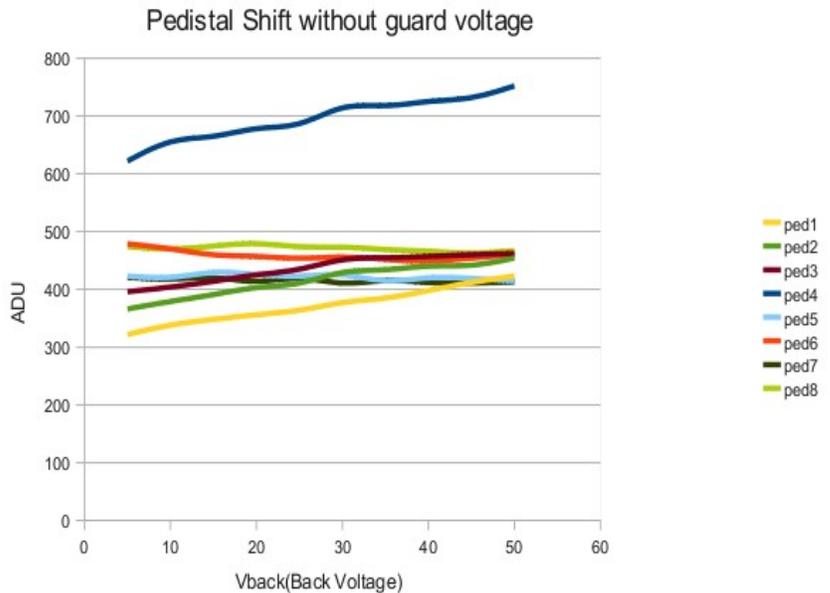


fig3. Pedestal Shift without guard Voltages

All 8 regions are analyzed for pedestal shifts. The test setup is as follows: no guard voltages is applied and back voltage is increased for every test and mean ADC values are recorded for all different regions. The fig.3 shows the 4th region without BPW layer, in which pedestals increase with increase of the back voltage. Also the overall increase of ADC values is seen, due to the back gate effect. Other regions show that the back-gate effect is eliminated by introduction of BPW layer. In Fig.3 the curves for region 1,2 and 3 are measured without guard voltages, which results in the increase of pedestal values. This is stabilized by applying guard voltage, as can be seen in fig4.

The test setup for fig4 is as follows:

- Integration time is 10us
- V_{back} is 5V with 10 steps
- Reset Voltage is 660mV
- Guard Voltage1 $V_{g1} = Gnd$
- Guard Voltage2 $V_{g2} = 1.8V$

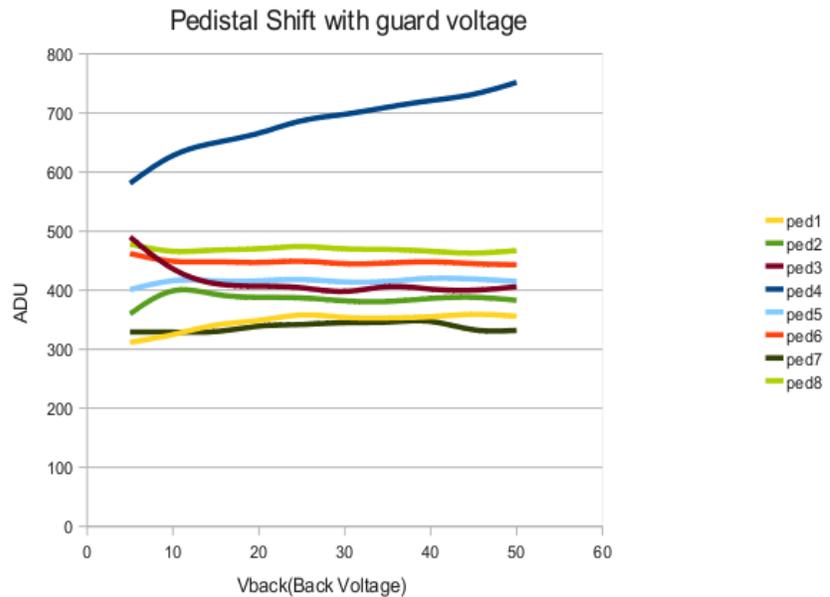


fig4. Pedestal Shift with guard Voltages

3. Dependence of the transistors characteristics on the back voltage:

INTPIX3 has transistor TEG (test element group) at the top and right side of the chip, with and without BPW, to evaluate BPW works. Fig5 shows INTPIX3 top layout with transistor location. 7 NMOS test transistor and 6 PMOS test transistor for both: with and without BPW.

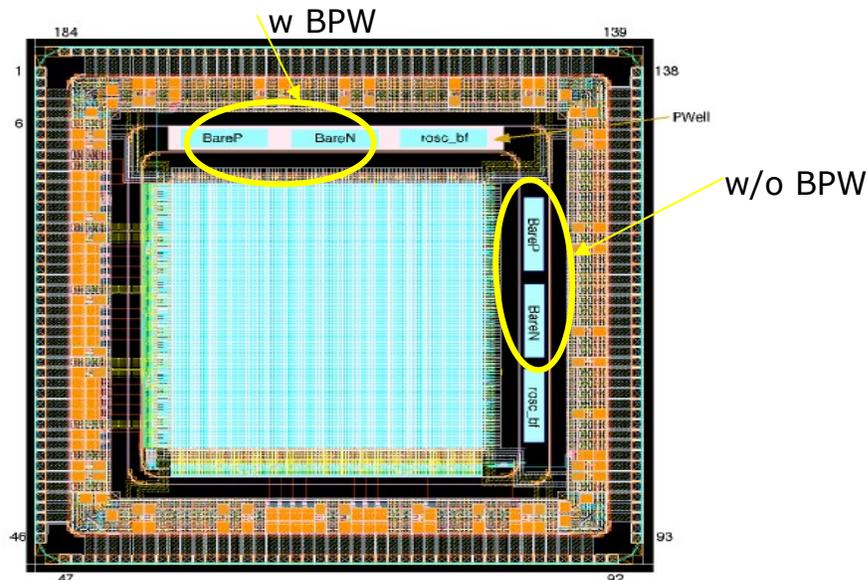


fig5. INTPIX3 layout with transistor location

1. **Without BPW** : The fig8 shows the transistor characteristic of NMOS transistor without BPW, where increase in back voltage result in change in threshold voltage. The maximum back voltage applied to this transistor is 100V, the breakdown voltage for INTPIX3 is 120V. The increase in back voltage effect the top electronics of the sensor which is nothing but back gate effect. After 50V the transistor are not operational.

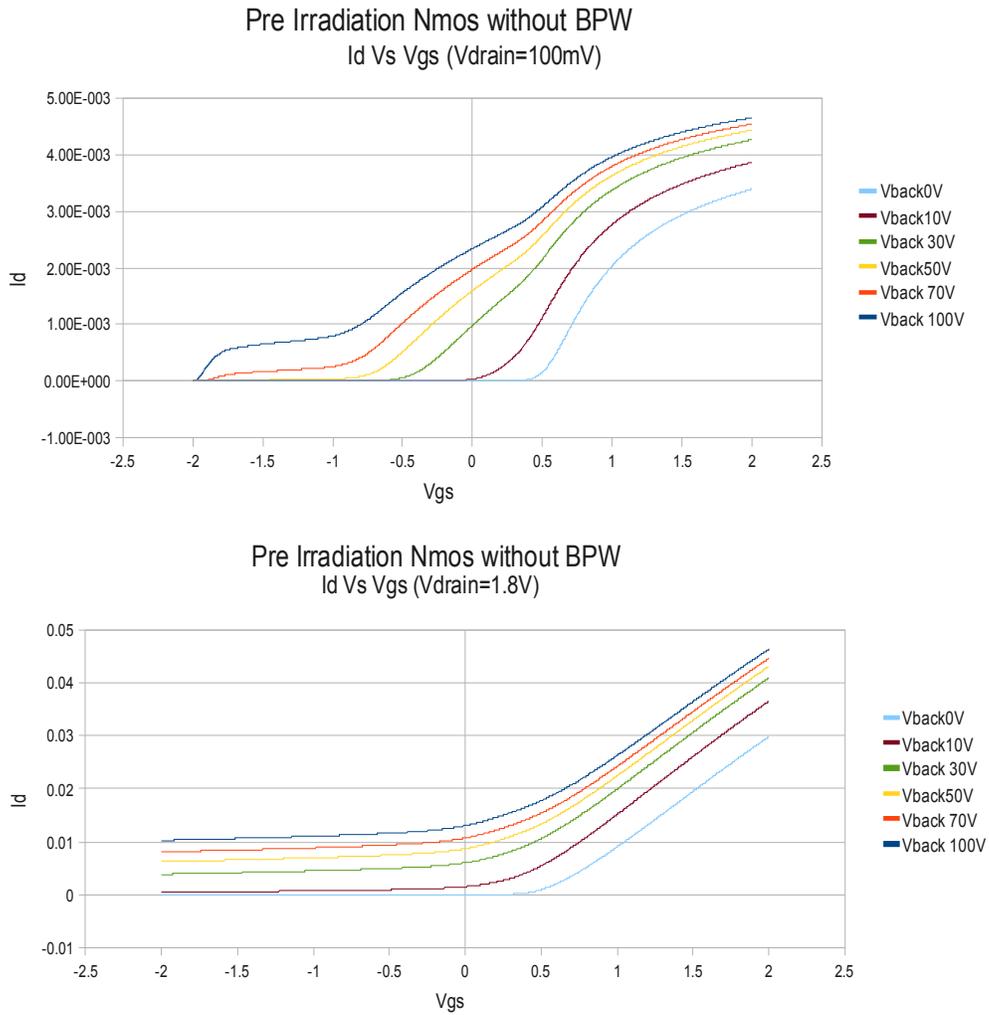


fig8: I_d vs V_{gs} without BPW $V_{drain}=100mV$ and $1.8V$ with $V_{guard1,2}=Floating$

2. **With BPW:** The fig9 and fig10 shows the transistor characteristic of NMOS with BPW. I_d vs V_{gs} curve is not effected by back gate voltage upto 100V and the role of guard voltage can be seen in fig10. This confirms the stabilization of back gate effect by introduction of BPW layer in the design.

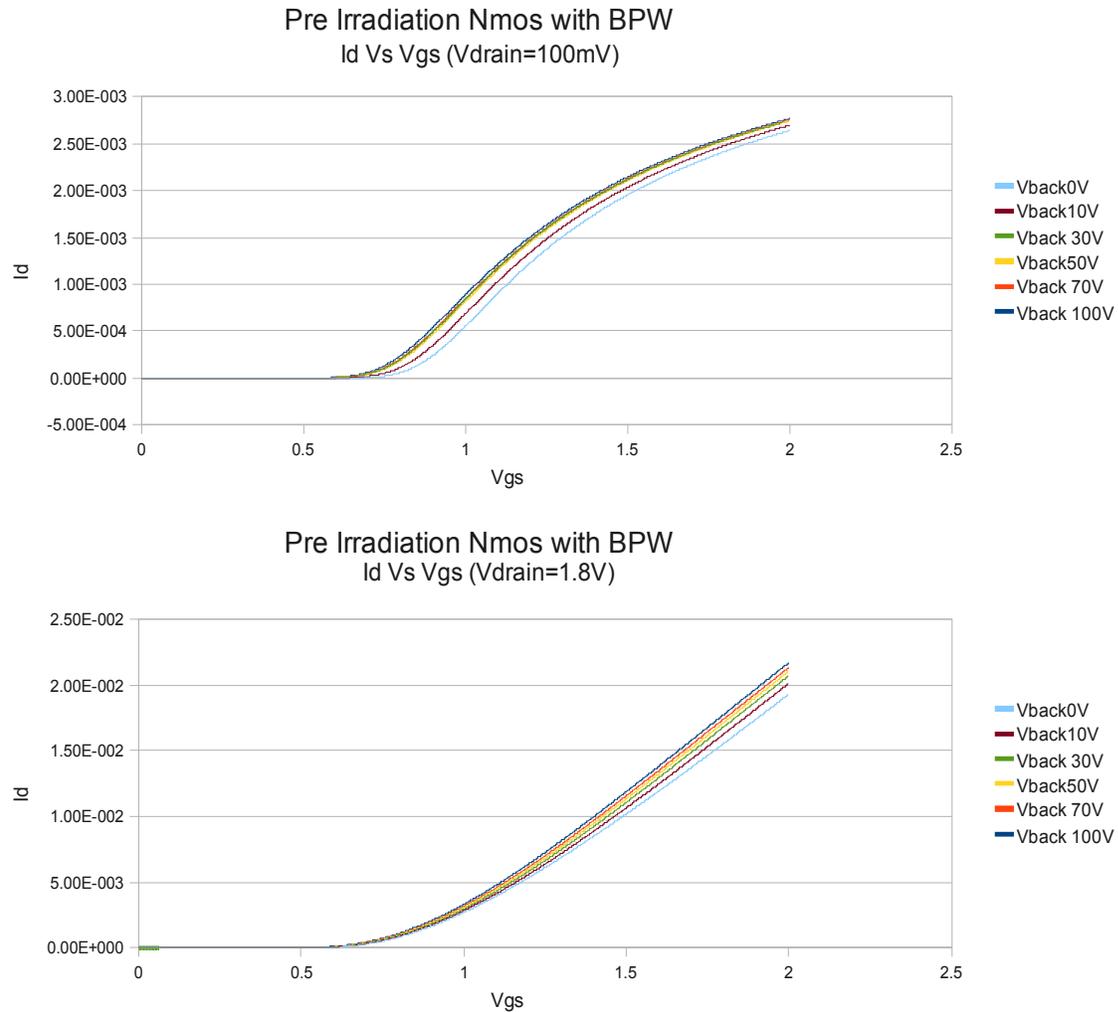


fig9: I_d vs V_{gs} with BPW $V_{drain}=100mV$ and $1.8V$ with $V_{guard1,2}=Floating$

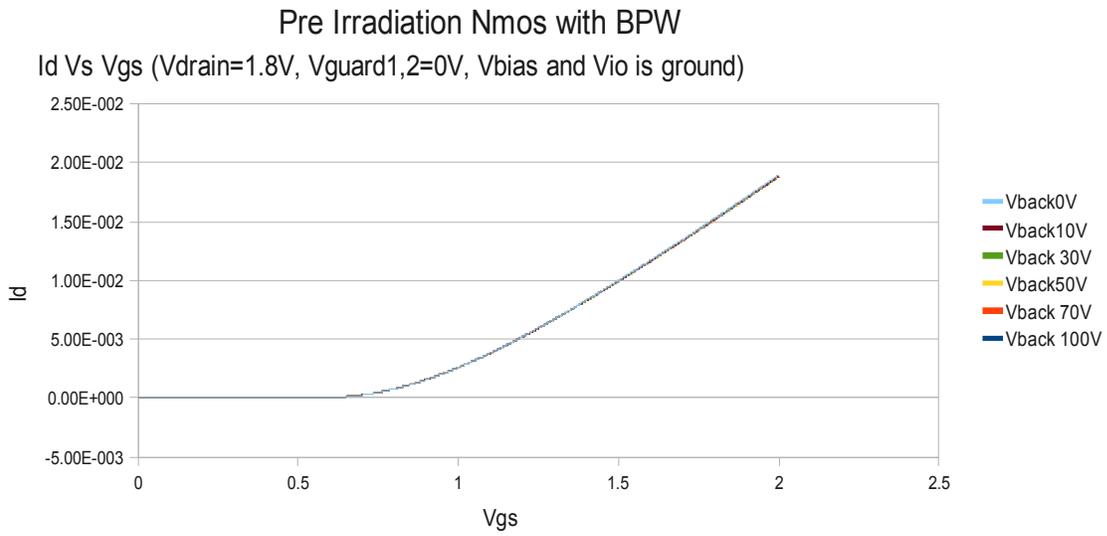
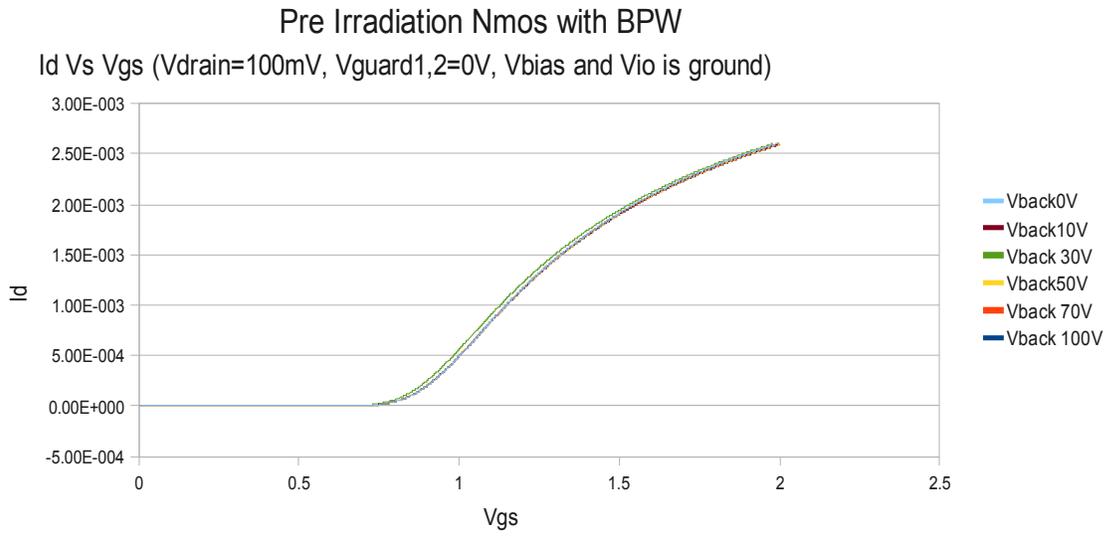


fig10: I_d vs V_{gs} with BPW $V_{drain}=100mV$ and $1.8V$ with $V_{guard1,2}=0V$

4. **Test of response of the detector to red light diode (650 nm):**

Fig11 visualize the image of red light laser diode illumination of whole detector. Red laser is impinging on the sensor at a distance of 20cm. As discussed earlier region 1,2 and 3 is provided with guard ring to isolate the edge of the wafer. This effect of no guard voltage and guard voltage can be seen in fig12 and fig13 respectively. The small part of the red laser spot is moves to the region 2 result in completely saturated region due to no guard voltage. The stabilize effect can be seen in fig13 where 1.8V of guard voltage is applied.

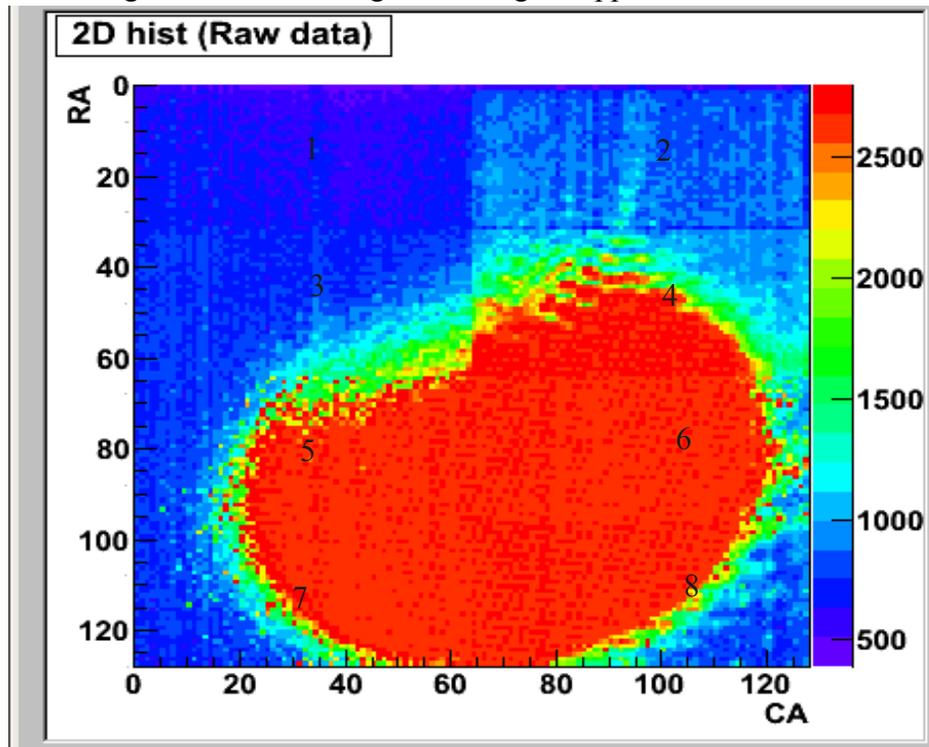


fig11: Red Light impinge on INTPIX3

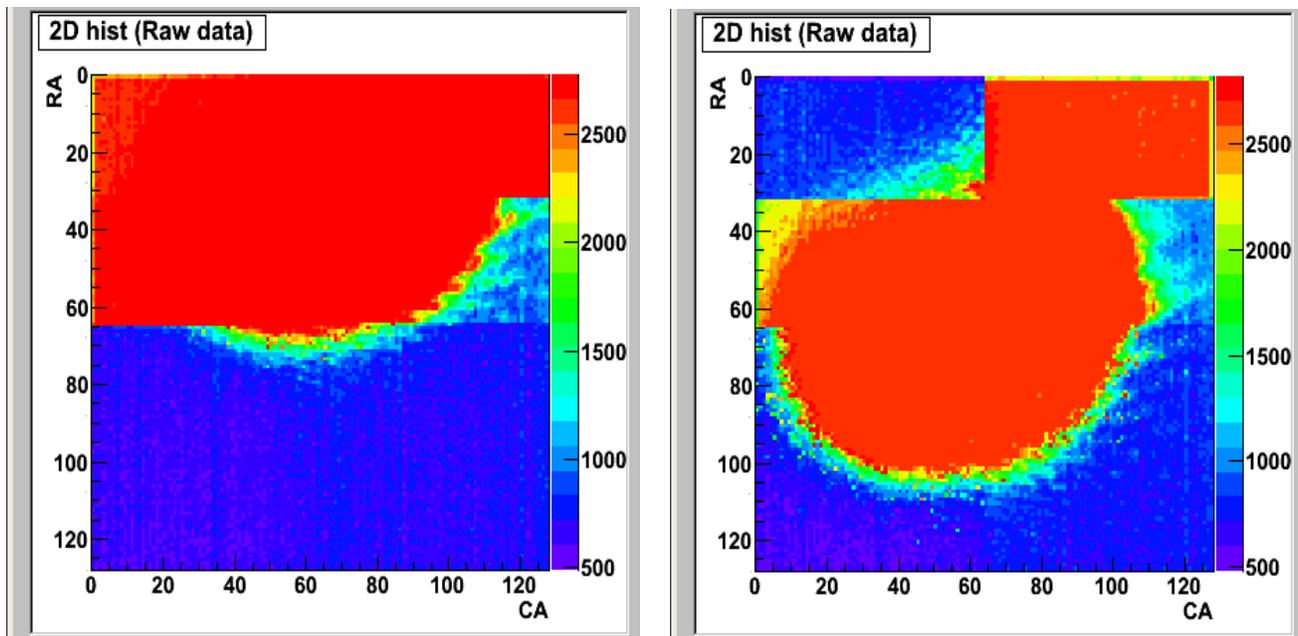


fig12: Red Light impinge on INTPIX3 and Saturation of region 1,2 and 3.

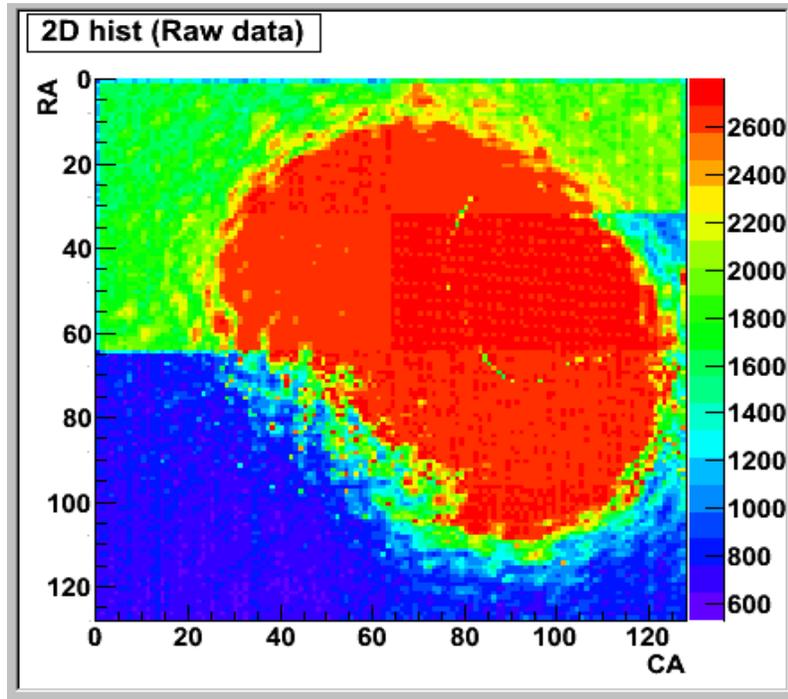


fig13: Application of guard Voltages

5. Irradiation of INTPIX3 with Americium Am-241:

Data from the detector tests with Americium source are analyzed with a set of macros written to read out root file generated by the readout board. The activity of Am-241 source is 10mCi(=370MBq). Whole test procedure is divided into two parts, one is without source (in darkness) and other is with the source illuminating the detector (also in darkness). As the incident photon rate of Am-241 is low, the source is kept close to INTPIX3 and the integration time was set to 0.5ms.

$V_{back}/RSTV$	Exposure Time	X-ray Source
100V/750mV	0.5ms /frm x 4900 frm	Am-241

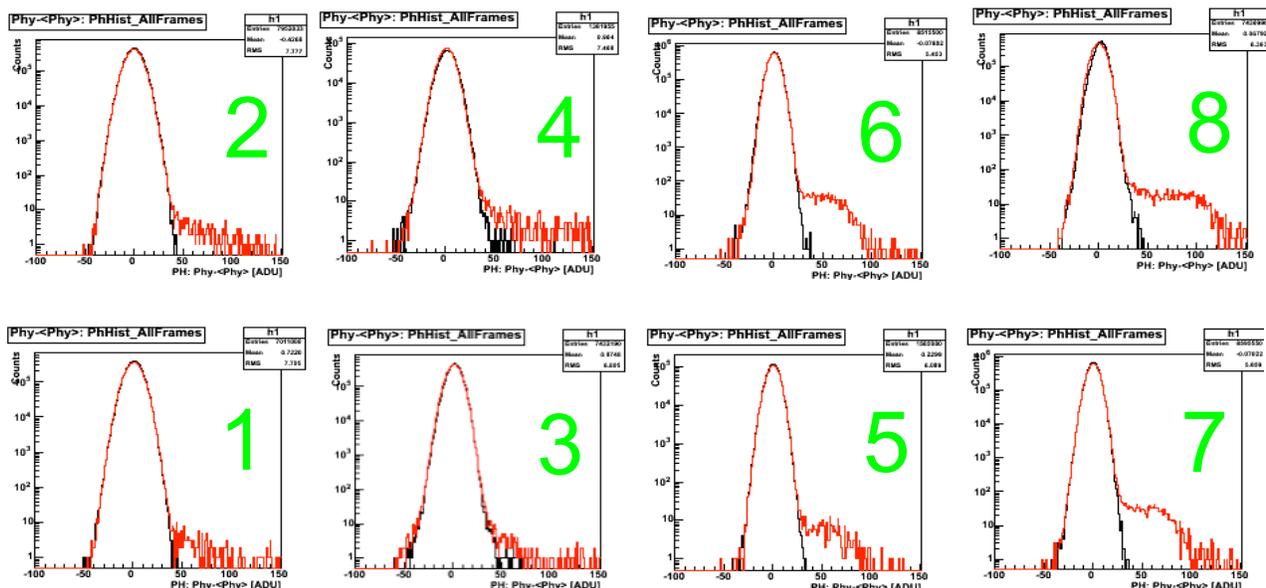


fig14: Am-241 with 4900 frames for all 8 regions of INTPIX3

The fig14 show two lines, black is for without source in dark and red is for with source in dark. The region 5,6,7 and 8 shows a right shoulder which is nothing but the Am-241 line of 13.9keV,.

Conclusion: Properties of the pixel detector prototype INTPIX3 have been determined by various tests and measurements performed, such as pedestal shifts, I_d vs V_{gs} characteristics, to evaluate effects of BPW on suppression of the back-gate effect. The guard-ring voltage effects were also studied. The irradiation of the detector with Am-241, which has 3 monochromatic gamma lines of 13.9keV, 26.3keV and 59.5keV, was done. The 13.9keV line is clearly seen in a simple ADC spectrum. Currently cluster analysis is attempted to observe higher energy lines.

References

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2. SOI Pixel Detector R&D <http://rd.kek.jp/project/soi/>
3. IEEE Nuclear Science Symposium, Conference record, N34-4, Oct. 29-Nov. 4, 2006, San Diego "Monolithic Pixel Detector in a 0.15um SOI Technology" Y. Arai, M. Hazumi, Y. Ikegami, T. Kohriki, O. Tajima, S. Terada, T. Tsuboyama,