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Readout electronics for LumiCal detector

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Abstract

The development of readout electronics for the luminosity detector (LumiCal) at the ILC, performed within the EUDET consortium, is presented. The LumiCal design impose several challanging constraints and requirements on the readout electronics system. The readout should work for a wide range of sensor capacitances, up to about 100 pF, and for a very wide dynamic range of input charge, from 2 fC to 10 pC. In addition it should be fast enough to separate events from the subsequent bunch crossings, dissipating very low power. The proposed LumiCal readout channel architecture comprises of two main ASICs i.e., the preamplifier-shaper and the analog-to-digital converter ASIC. For later integration in the complex multichannel readout system several peripherial circuits (DACs, differential I/O, reference voltages) are also necessary. The above mentioned components of the readout system were designed, the prototypes were produced and subsequently tested. The prototypes were fabricated in 0.35 μm CMOS technology. The prototypes of all circuits are fully functional and the quantitative measurements performed so far confirm a good agreement with simulations. In this report the design and measurements results of the produced prototype ASICs are discussed.

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1 Introduction

The measurement of luminosity in the future International Linear Collider (ILC) will be done by Si/W sandwitch calorimeter called LumiCal [1]. The operational conditions of the LumiCal detector regarding signal dynamic range, noise, event rate, hit occupancy and sensor granularity (and so its capacitance) set strong requirements on the readout electronics. The development of the readout electronics infrastructure fulfiling the LumiCal specifications is supported by the European Community under the EUDET project [2].
The detailed discussion of the LumiCal detector structure and the resulting constraints on the readout electronics architecture was given in the previous report [3]. Here we summarize the most important requirements and constraints:

- front–end electronics works in two modes: in the physics mode it is sensitive to signals from electromagnetic showers resulting in high charge depositions up to 10 pC per single sensor pad; in the calibration mode it detects signals from the minimum ionizing particles (MIP most probable deposited charge 4fC),
- signal to noise ratio (S/N) should be at least 10,
- very wide pad capacitance range 10 pF – 100 pF, resulting from sensor geometry,
- front–end electronics should be fast enough to resolve signals from subsequent beam bunches which are separated in time by about 350 ns,
- reconstruction procedure needs more then 8 bit ADC precision on the measurement of the deposited energy,
- power dissipation requirements (not yet precisely defined but of the order of some mW per channel) may be strongly relaxed if the power switching off is implemented between bunch trains (in the ILC after each 1 ms bunch train there will be about 200 ms pause).

Taking into account above specifications the readout chain architecture has been proposed as shown in fig. 1. The two main dedicated ASICs in the signal processing chain are the front-end electronics ASIC, containing preamplifier-shaper circuits, and the analog-to-digital conversion (ADC) ASIC. The digital data should be collected by the data concentrator with optical driver circuits. In the following we report on the design and measurements of the prototype front–end and ADC ASICs, including some specific peripheral circuits needed in the multichannel readout system.

2 Front-end electronics development

The detailed discussion of the front-end electronics design and measurements was given in [3, 4]. Here only a short summary is given.

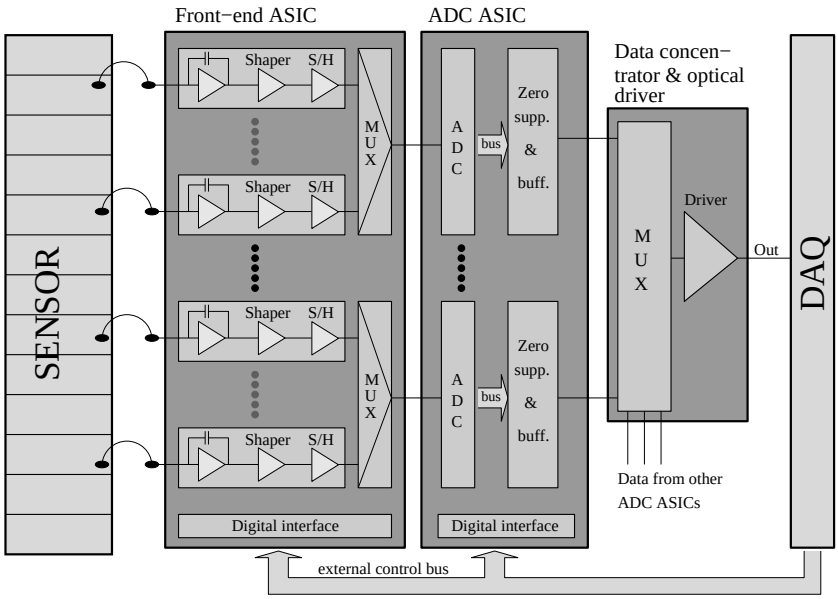

Figure 1: Block diagram of the LumiCal full readout chain

2.1 Front-end electronics design

The proposed front–end architecture comprises switched-gain charge preamplifier, pole-zero cancellation circuit (PZC) and switched-gain 1st order shaper (fig. 2). The preamplifier works for a wide range of input capacitance values up to above 100 pF. The input charge dynamic range (summed over the calibration and physics mode) from 2 fC to 10 pC covers more than 3 orders of magnitude. The circuit has to be fast with a peaking time of about 70 ns.

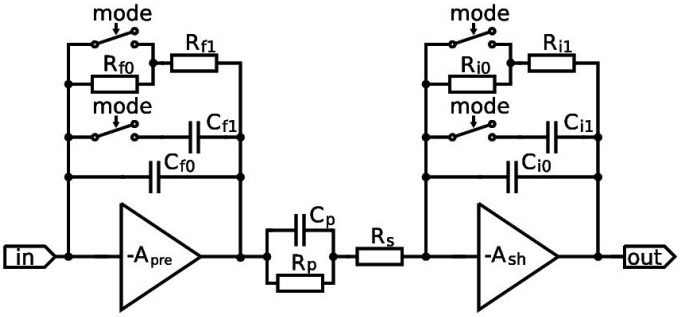

Figure 2: Block diagram of the single front–end channel

Assuming high enough open loop gain of the preamplifier (A_{pre}) and the shaper amplifier (A_{sh}), the front-end transfer function is given by:

$$\frac{U_{out}(s)}{I_{in}(s)} = \frac{1}{C_f C_i R_s} \cdot \frac{s + 1/C_p R_p}{s + 1/C_f R_f} \cdot \frac{1}{(s + 1/C_i R_i)(s + 1/C_p(R_p||R_s))} \tag{1}$$

and may be simplified (assuming $C_f R_f = C_p R_p$) to a standard first order CR–RC shaping.

2.2 Front-end electronics measurements

A prototype ASIC containing eight front-end channels was designed and fabricated in 0.35 μm CMOS technology. The ASIC consumes about 8.9 mW per channel. The results of measurements showing the pulse response in physics mode, the gain in physics mode and the Equivalent Noise Charge (ENC) in both physics and calibration mode, are shown in fig. 3 and fig. 4

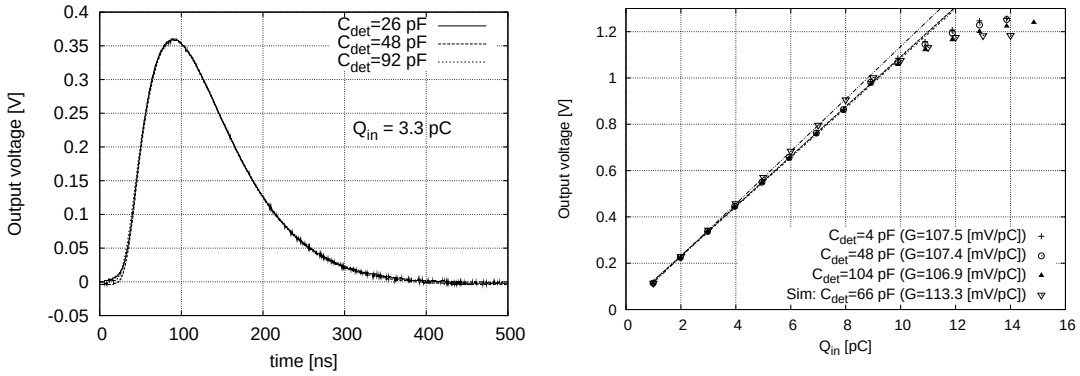

Figure 3: Output pulses in physics mode (left), gain in physics mode (right)

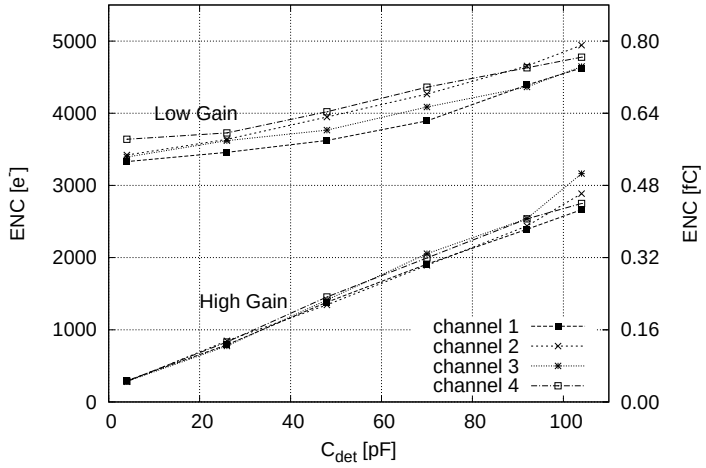

Figure 4: Noise ENC measurements in physics mode (low gain) and calibration mode (high gain)

The measurements are in good agreements with simulations. Some of the important measured parameters are given in the table 1.

Table 1: Front-end electronics parameters

Mode	Gain [mV/fC]	Noise@50pF [fC]	Max charge [pC]	Max rate [MHz]	Crosstalk [%]
Physics	0.107	0.62	10	3	≈1
Calibration	≈20	0.28	0.035	3	≈0.1

3 Development of 10 bit pipeline ADC

The detailed discussion of the ADC design and the measurements results obtained with the first prototype of the ADC main blocks, were given in [3]. In the following we briefly summarize the design of the complete ADC and present the measurements results of the second prototype [5].

3.1 ADC design

The key ADC specifications are:

- 10 bit resolution
- sampling frequency in the range 3-25 MHz (final choice will depend on number of front-end channels per ADC)
- ADC versions with and without sample and hold (S/H) stage (no decision is taken yet whether the S/H will be part of the front-end or ADC)
- power efficient, possibility of power switching ON/OFF

To fulfill these requirements a 10 bit pipeline ADC with 1.5-stage architecture was chosen. A fully differential pipeline ADC was implemented with input sample and hold stage followed by 9 pipeline stages (1.5 bit per stage) and containing digital correction block (fig. 5). The second prototype is an extension of the first one which contained only the 8 pipeline stages. In addition the second prototype contains also the clock and power switching circuitry. Only the biasing and reference voltages need to be applied externally.
The main components of pipeline stage (shown in fig. 5, right) are: a fully differential amplifier and a dynamic latched comparator (fig. 6). The sample and hold stage uses the same amplifier as the pipeline stages.

3.2 ADC measurements

The prototype ASIC containing the ADC channels with and without S/H input stage was designed and fabricated in 0.35 μm CMOS technology. The photograph of the prototype is shown fig. 7.

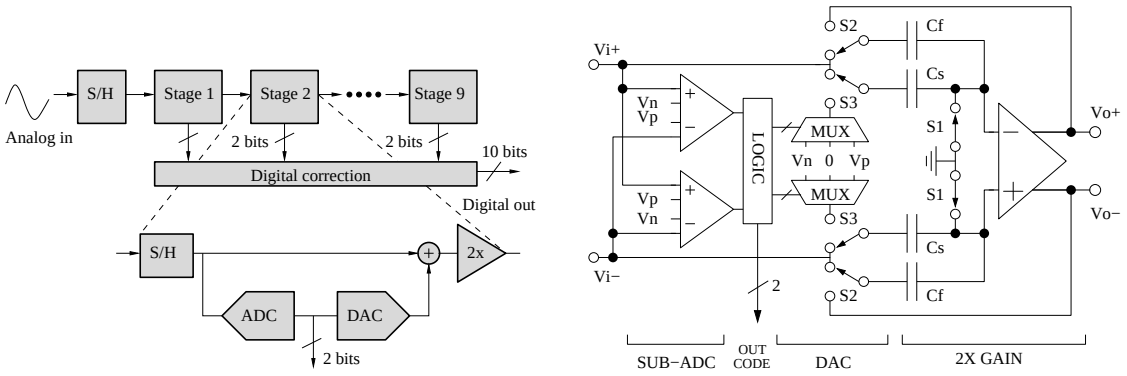

Figure 5: Pipeline ADC architecture (left), single pipeline stage (right)

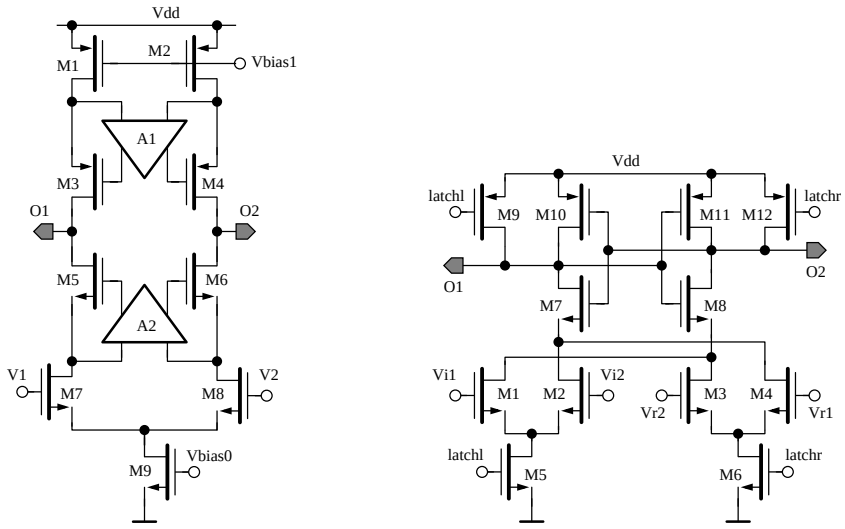

Figure 6: Schematic diagram of fully differential amplifier with boosted gain (left), schematic diagram of the latched comparator (right)

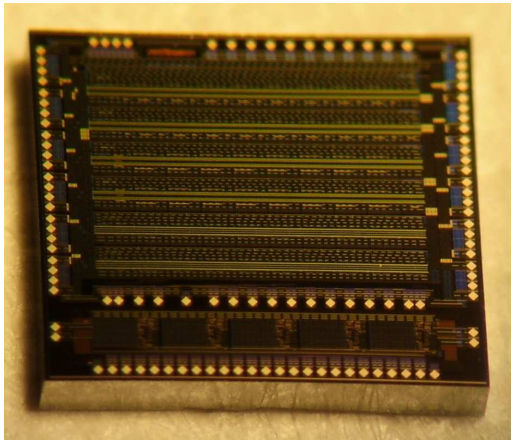

Figure 7: Photograph of ADC prototype

3.2.1 Test Setup

To measure the ADC parameters an updated version of the test setup, described in [3], was prepared. The block diagram of the setup is shown in fig. 8.

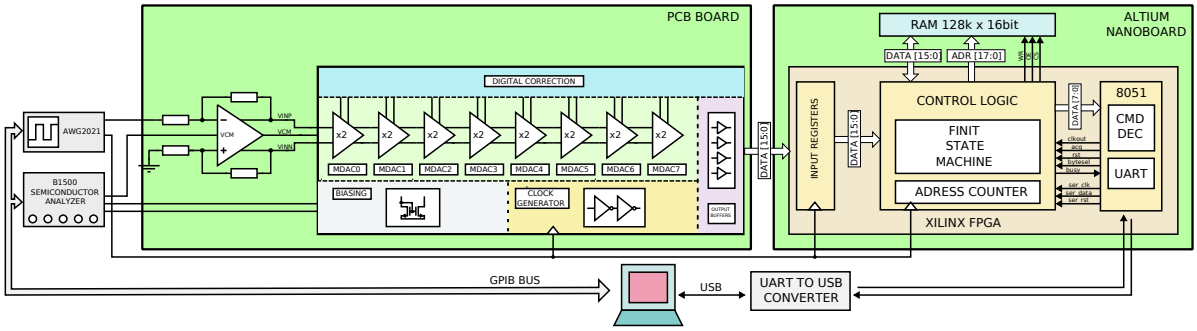

Figure 8: Block diagram of the complete test system

The main setup components are:

- Signal sources for static (Agilent B1500) and dynamic (Tektronix AWG2021 or AFG3102 generator) measurements
- External single-ended to differential converter
- FPGA based (Altium nanoboard with Xilinx Spartan2E) data acquisition system
- PC computer

3.2.2 Measurements

The full ADC functionality was confirmed by measurement of the transfer function shown in fig. 9.

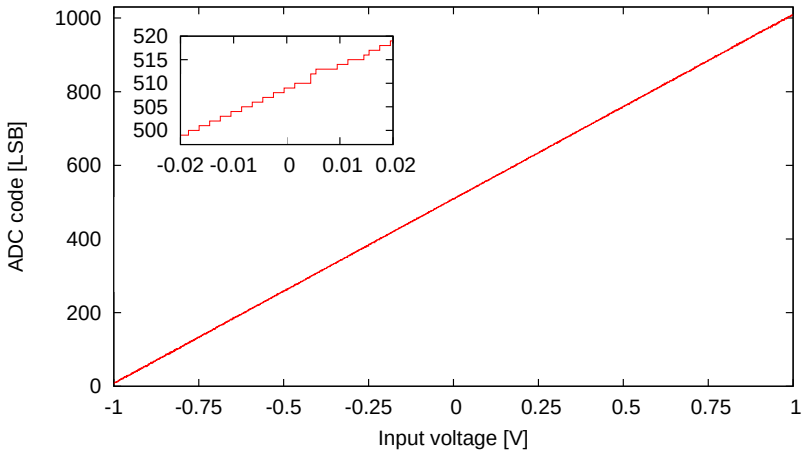

Figure 9: Static measurement of ADC transfer function

To characterize static behaviour the linearity measurements were performed for the ADC versions with and without the S/H stage. The resulting integral (INL) and differential (DNL) nonlinearities ares shown in fig. 10.

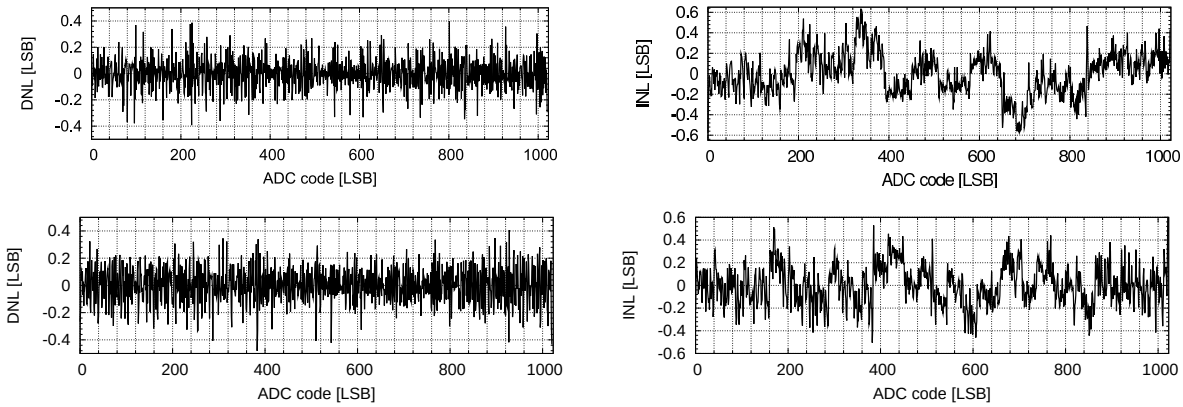

Figure 10: Static measurements of INL and DNL errors for ADC with S/H stage (upper plots) and without S/H stage (lower plots)

Both ADC versions show good differential ($DNL < 0.5$ LSB) and integral ($INL <$ 1 LSB) linearity.
The dynamic ADC performance was investigated with sinusoidal wave input signal and using Fast Fourier Transform to calculate the output signal spectrum. From this spectrum all dynamic parameters i.e., Signal to Non Harmonic Ratio (SNHR), Spurious

Free Dynamic Range (SFDR), Total Harmonic Distortion (THD) and Signal to Noise and Distortion Ratio (SINAD) are calculated. A typical result of such measurement is shown in fig. 11. It is seen that the SNHR equals 58.5 dB what corresponds to about

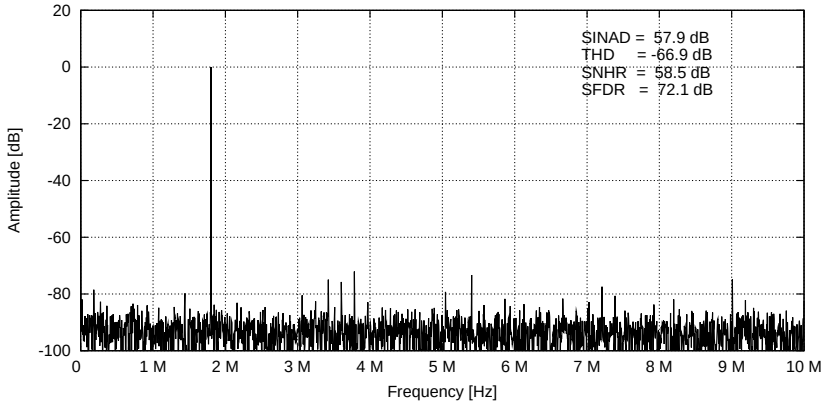

Figure 11: Example of FFT measurement with f_{in}=1.8 MHz and f_{clk}=20 Mhz

9.5 bit resolution.
The dependence of dynamic ADC parameters versus sampling frequency was also investigated. The results of such measurements are shown is fig. 12. The measurements

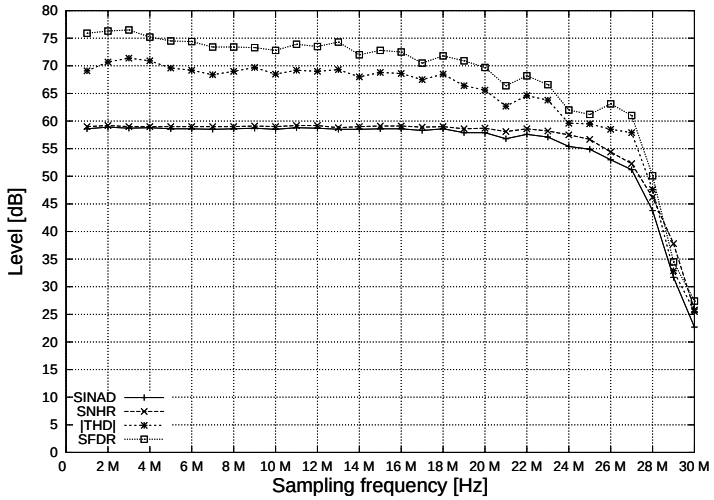

Figure 12: ADC performance as a function of sampling rate

shown in fig. 12 were done for the input signal frequency equal to about 10% of the sampling frequency. It is seen that the ADC is fully functional and sustains the resolution of about 9.5 bit for a wide sampling frequency range. The resolution drops below 9 bit for sampling frequencies above 25 MHz.
Since the presented ADC should work for a wide range of sampling frequencies the ADC power consumption and its scaling with sampling frequency is of particular im-

portance. Preliminary estimation of power consumption versus sampling frequency was done measuring, for a given sampling frequency, the ADC linearity patameters (INL, DNL) versus the power consumption. The minimum power consumption, for a given sampling frequency, was taken requiring small enough nonlinearities ($INL \leq 1$ LSB, $DNL \leq 0.5$ LSB). The results of such measurements for the ADC prototypes with and without S/H stage are shown in fig. 13. It is seen that the power consumption

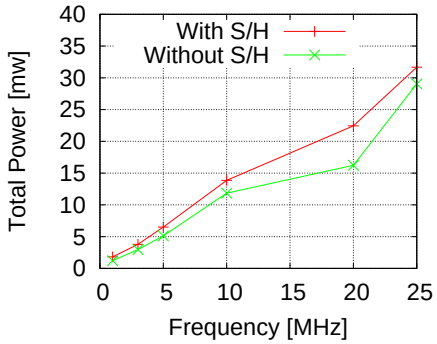

Figure 13: ADC total power consumption as a function of sampling frequency

scales linearly with the sampling frequency. Since the measurements were done with the static inputs the absolute values may be slightly underestimated. To account for dynamic effects few dynamic measurements were done for input frequency equal half of the sampling frequency (Nyquist frequency). In such cases a good ADC performance was obtained for slightly higher power consumption. The power consumtion normalized to sampling frequency in these worst case conditions was of about 1.5 mW per 1 MHz.

4 Peripheral circuits development

Apart from the front-end and ADC ASICs some other circuits, necessary in complex multichannel readout system, were studied, designed and fabricated. These circuits are:

- Low-power small-area high-swing digital to analog converter (DAC), to control various analog parameters,
- Low-power voltage bandgap reference and temperature sensor, for precise biasing and temperature measurements,
- High-speed low-voltage differential signalling (LVDS) transmitter and receiver circuits, for digital I/O.

The first prototypes of the above circuits were fabricated in 0.35 μm CMOS technology.

4.1 Development of 10 bit DAC

The 10–bit DAC design is based on a current steering architecture. The detailed discussion of the DAC design and measurements is presented in [6], here only a short summary is given. The core DAC component, shown in fig. 14 (left), is a binary weighted 9–bit current sources matrix with the active cascode stages. A 10–bit resolution is achieved by mirroring (fig. 14, right) the current from the 9–bit current sources matrix and switching (with an MSB switch) between the current source or sink at the input to the high–swing output amplifier. To obtain high output swing and high current drive capability, a class AB rail-to-rail output transimpedance amplifier was designed.

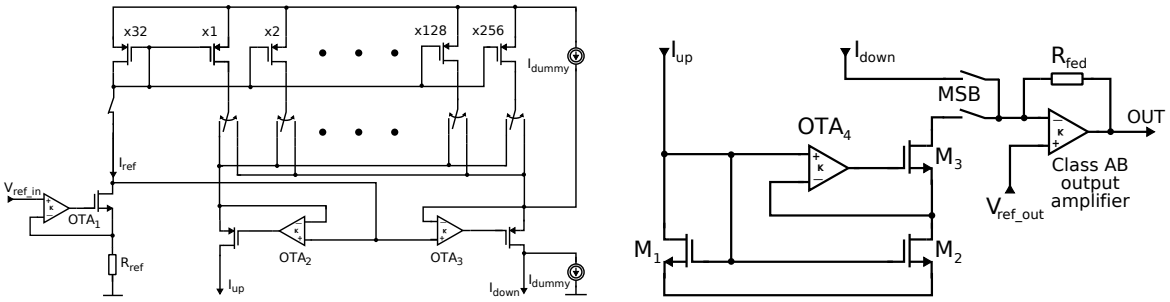

Figure 14: Block diagram of the DAC current source matrix and active cascode stages (left), block diagram of current mirror and high–swing output amplifier (right)

The designed ASIC occupies 0.18 mm^2 area. The measurements showed that the power consumption is below 0.6 mW. The DAC was found fully functional as seen on the measured transfer function (fig. 15, left) and shows very good integral and differential linearity (fig. 15, right).

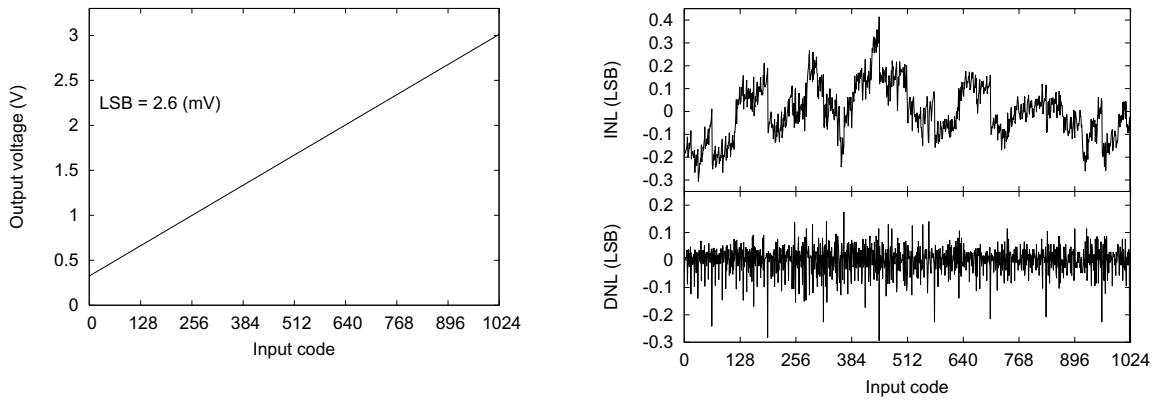

Figure 15: DAC transfer function (left), measured INL and DNL nonlinearities (right)

The measurements performed on few prototypes demonstrated that the maximum values

of INL and DNL are below 0.42 LSB. The effective number of bits calculated from the static measurements equals 9.85.

4.2 Voltage reference and LVDS circuits

The voltage bandgap reference and temperature sensor circuits [7], and the fast LVDS transmitter [8] and receiver [9] circuits were designed and the first prototypes were fabricated. The measurments of these ASICs have just started. No precise quantitative results are available but the full functionality of both ASICs was verified.
Regarding the voltage reference ASIC, it was measured that the bandgap reference voltage value is equal 1214 mV and changes only by about 1 mV for the temperature range 20–100 degree. It was also verified that the temperature sensor output changes by about 200 mV in the same temperature range.
Reagarding the LVDS ASIC, an example measurement of the transmitter signals is shown in fig. 16. It is seen that both output phases respond correctly with the amplitudes of

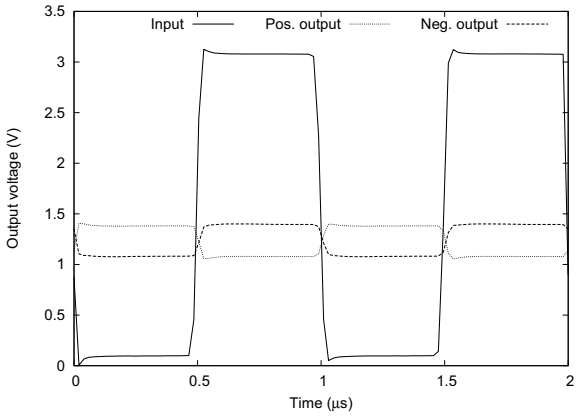

Figure 16: Measurement of LVDS transmitter operation

about 350 mV, in agreement with simulations. Also the DC output level of about 1.2 V agrees with simulations.

5 Conclusion

Within the EUDET project all important components of the readout electronics for the LumiCal are designed fabricated and tested.
Regarding the front-end electronics ASIC the electrical tests are completed and the prototype is ready to be integrated with the sensor in order to test the detection chain comprising the sensor, the fanout and the front-end electronics. After the integration, which is in progress now, and verification of such readout chain the front-end ASIC will be used on the test beam.

The development of 10 bit pipeline ADC was done in two design and prototyping stages. The second prototype contains all ADC functional blocks. The measurements of this prototype are still in progress but the results obtained by now confirm the full functionality of the ASIC. In particular the obtained resolution of about 9.5 bit and the operational frequency range up to about 25 MHz fulfill the requests. Among the tests still to be completed are the power switching ON/OFF functionality, power scaling measurements and cleaning the setup from external harmonic distortions which impede the measurements of a pure ASIC distortions. After the completion of the tests the next development step will be the extension of the present ADC design to a multichannel version. This would allow to integrate the ADC in the multichannel readout system.
Apart from the front-end and ADC ASICs the low-power DAC ASIC, the voltage bandgap reference and temperature sensor ASIC, and the fast LVDS transmitter and receiver ASIC were designed, fabricated and partially tested. These ASICs were designed in view of being used in a multichannel readout system. The performed tests showed that all of them are fully functional. The DAC measurements are already succesfully completed while the other two ASICs still need more quantitative tests to be done.
Summarizing, the prototypes of all important components of the LumiCal readout electronics are found fully functional and ready for the integration in the multichannel readout system.

Acknowledgement

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